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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,512	08/31/2001	Yasuo Osone	500.40530X00	8183

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EXAMINER	
GRAYBILL, DAVID E	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 05/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/943,512	OSONE ET AL.	
	Examin r	Art Unit	
	David E Graybill	2827	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *14-24,26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The drawings were received on 2-27-4. These drawings are not acceptable.

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 10A and 10B. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Figures 3, 4, 10 and 11 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 26 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at

the time the application was filed, had possession of the claimed invention. The undescribed subject matter is the negative limitation, "wherein emitter electrodes disposed at both ends of the group are not located over the areas which the through holes in the wiring board occupy."

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 26 is rejected under 35 U.S.C. § 112, first and second paragraphs, as the claimed invention is not described in such full, clear, concise and exact terms as to enable any person skilled in the art to make and use the same, and for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The unenabled and indefinite claim language is the limitation, "wherein emitter electrodes disposed at both ends of the group are not located over the areas which the through holes in the wiring board occupy." To further clarify, it is inherent that there is a frame of reference wherein the emitter electrodes disposed at both ends of the group are located over the areas which the through holes in the wiring board occupy.

Also, in claim 26 there is insufficient antecedent basis for the language "both ends of the group."

Claim 27 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 27 there is insufficient antecedent basis for the language "both ends of each group."

Claim 26 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejections supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Also see In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 14-23 are rejected under 35 U.S.C. 102(a) as being anticipated by Shirakawa (EP1077494).

At column 10, line 15 to column 11, line 35; column 18, line 9 to column 20, line 6; and column 22, line 52 to column 23, line 7, Shirakawa discloses the following:

A multilayer wiring board 12, 13 having through holes 10b in a thickness-wise direction, wherein a semiconductor substrate 1 mounted on the multilayer wiring board has through holes 10 in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate are included in areas, which the through holes in the multilayer wiring board occupy, wherein conductive layers 11 are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material, wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material, wherein wirings 11, which connect

heating areas in the semiconductor substrate mounted on the multilayer wiring board, are electrically connected to the through holes in the semiconductor substrate, and electrical connection is effected through the heating areas, the wirings, the through holes of the semiconductor substrate, the through holes of the multilayer wiring board, and a surface of the multilayer wiring board, on which the semiconductor substrate is not mounted, in this order..

A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has through holes in a thickness-wise direction thereof, and wherein the through holes in the semiconductor substrate are located relative to the through holes in the multilayer wiring board so that entire areas, which the through holes in the semiconductor substrate occupy, in a plane orthogonal to the thickness-wise direction of the multilayer wiring board and of the semiconductor substrate partly (in some measure or degree) overlap areas which the through holes in the multilayer wiring board occupy, wherein conductive layers 11 are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material, wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

A multilayer wiring board having a cross-plane through hole or holes, wherein an in-plane location of respective heat dissipating regions in a semiconductor substrate mounted on the multilayer wiring board is inside of a through hole or an area where through holes are built in the multilayer wiring board, wherein conductive layers 11 are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material, wherein a semiconductor element is mounted, in which conductive layers are formed on side surfaces of the through holes, or interiors of the through holes comprise a conductive material.

A multilayer wiring board having through holes in a thickness-wise direction, wherein a semiconductor substrate mounted on the multilayer wiring board has cross-plane through holes, and heat flows one-dimensionally through the through holes in the semiconductor substrate and the cross-plane through holes in the multilayer wiring board when heat flows out to a surface of the multilayer wiring board opposite to that surface thereof, on which the semiconductor substrate is mounted, via the through holes in the semiconductor substrate and the through holes in the multilayer wiring board.

A multilayer wiring board having cross-plane through holes, wherein in-plane distribution of heat dissipated from a transistor or transistors of a

semiconductor substrate mounted on the multilayer wiring board substantially coincides with distribution of the through holes.

A multilayer wiring board having cross-plane through holes, wherein in-plane distribution of heat dissipating from a transistor or transistors of a semiconductor substrate mounted on the multilayer wiring board substantially coincides with in-plane distribution of large and small cross-sections areas of the through holes.

A wiring board, wherein a semiconductor substrate having cross-plane through holes, which are connected to emitter wirings 11 connected to emitters 1 of heterojunction bipolar transistors and extended through the semiconductor substrate and which have conductive layers on sides thereof or inside thereof, is mounted on the multilayer wiring board, and the cross-plane through holes in the semiconductor substrate and through holes extending through the wiring board are connected to each other, and wherein conductive layers are provided on sides of or inside of the connected through holes in the semiconductor substrate and the wiring board, and in-plane areas, which the through holes in the semiconductor substrate occupy, in a plane of the multilayer wiring board and of the semiconductor substrate are included in areas which the through holes in the multilayer wiring board occupy.

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claim 24 is rejected under 35 U.S.C. 102(a) as being anticipated by applicant's admitted prior art.

In the specification, at pages 12-22, applicant discloses as prior art a semiconductor device including a plurality of finger-shaped emitter electrodes 7 or source electrodes, and at least one via hole 5 which are arranged in rows in a first direction on a semiconductor substrate, wherein the emitter electrodes or the source electrodes are connected to a conductive layer 6 formed on a back surface opposite to a surface, on which the electrodes are formed, through the via hole, and wherein said rows comprising the emitter electrodes or source electrodes, and the via holes are arranged in parallel in a second direction orthogonal to the first direction, and the via holes are positionally shifted (in the second direction) from one another in adjacent rows among said rows, or adjacent rows are positionally shifted from one another in the first direction.

Claim 27 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Claim 25 is allowed.

Applicant's amendment and remarks filed 2-17-4 and 3-5-4 have been fully considered, are addressed by the rejections supra, and are further addressed infra.

Applicant contends that Figures 5 and 8 provide support for the limitation, "wherein emitter electrodes disposed at both ends of the group are not located over the areas which the through holes in the wiring board occupy."

This contention is respectfully traversed because Figures 5 and 8 are not limited to an absolute frame of reference or otherwise limited to a particular orientation, and it is inherent that there is a frame of reference wherein the emitter electrodes disposed at both ends of the group are located over the areas which the through holes in the wiring board occupy.

Also, applicant argues that Shirakawa does not disclose "any detailed arrangement of a wiring board side."

This argument is respectfully traversed because, as explicitly and clearly applied in the rejection, Shirakawa discloses a wiring board 12, 13, and all of the allegedly claimed "detailed arrangement."

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Customer Service whose telephone number is 571-272-2815.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
6-May-04